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(54) **Oscillation circuits**

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Circuits oscillateurs

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Description

The present invention relates to an oscillation circuit using an oscillator composed of a quartz oscillator or a ceramic oscillator as an oscillation source.

GB-A-2 040 633 describes an oscillation circuit which includes a quartz oscillator, a docked inverter controlled to operate for a predetermined period of time after oscillation begins, an input and an output of which are connected across the oscillator, and an inverter having an input and an output connected across the oscillator.

US-A-4 255 723 describes the insertion of a PMOS and an NMOS transistor in an inverter connected across an oscillator.

Fig. 1 of the accompanying drawings shows a conventional oscillation circuit using an oscillator. An oscillator 81 which is composed of a quartz oscillator or a ceramic oscillator, an inverter 82 and a feedback resistor 83 are connected in parallel. A capacitor 84 is connected between the earth voltage Vss and one terminal of the oscillator 81 and a capacitor 85 is also connected between the earth voltage Vss and the other terminal of the oscillator 81.

In general, with the above oscillation circuit, an oscillation start time is shortened and an oscillation start voltage is lowered if a large value of mutual conductance gm of the inverter 82 is set. As a result, the inverter 82 can be operated by a low voltage, for example, almost 3V. However, a penetrating current, i.e., a current which flows through the inverter 82 from the power source voltage Vcc to the earth voltage Vss is increased when the oscillation circuit is in oscillation operation near the operating point so that it is difficult to obtain a low consumption current with the above oscillation circuit.

As shown in Fig. 2, another conventional oscillation circuit may be arranged such that a clocked inverter 86 is connected in parallel with the inverter 82. In the oscillation circuit in Fig. 2, both the inverter 82 and the clocked inverter 86 are operated to cause the oscillation until the oscillation begins. The clocked inverter 86 is turned off after a predetermined time period has elapsed from the beginning of the oscillation, and thereafter the oscillation operation is maintained only by the inverter 82. Thus both short oscillation start time and low current consumption can be realized by the above circuit.

However, when the oscillation circuit is operated by the low voltage such as almost 3V, the operating point of oscillation of the inverter 82 is (1/2)Vcc, i.e., 1.5V where Vcc is the power source voltage. Generally, when the inverter 82 is embodied by means of the CMOS technique, it is constructed by connecting serially both the source-drain connections of P-channel MOS transistor and N-channel MOS transistor between the power source voltage Vcc and the earth voltage Vss, as shown in Fig. 3. A threshold voltage Vth of the MOS transistor is a typical parameter which has an influence upon the characteristics of both MOS transistors. The absolute value of the threshold voltage Vth is ordinarily set at about 1V. At that time, the current Icc flowing at the operating point of the CMOS inverter is given by following proportional expression as

$$Icc \propto (V_{GSN} - V_{thN})^2 \quad (1)$$

where V_{GSN} is a gate-source voltage of the N-channel MOS transistor shown in Fig. 3, and V_{thN} is a threshold voltage of the same.

However, the difference between the gate-source voltage V_{GSN} and the threshold voltage V_{thN} is reduced when the power source voltage Vcc is lowered. As a result, the variation of the current Icc is increased due to the variations of the power source voltage Vcc and the threshold voltage V_{thN}. For example, when $V_{thN} = 0.9 \pm 0.3V$ and $Vcc = 3 \pm 0.3V$, a ratio of maximum value Icc (MAX) and minimum value Icc(MIN) is given by following equation.

$$\frac{Icc(MAX)}{Icc(MIN)} = \frac{\{(3.3/2) - 0.6\}^2}{\{(2.7/2) - 1.2\}^2} = 49 \quad (2)$$

There is a difference of 49 times between the maximum and the minimum values of the operating currents. Assume that the operating current Icc required to maintain the oscillation is, for example, 100 μA, so much current of 4.9 mA flows at maximum owing to the variations of the power source voltage Vcc and the threshold voltage V_{thN}.

Accordingly, even if it is tried to lower the consumption current with the oscillation circuit in Fig. 2, the variations of the operating currents are increased when the circuit is operated by the low power source voltage and thus the low consumption current cannot be attained by this circuit. In other words, the oscillation circuit of Fig. 2 can both shorten the oscillation start time, and also lower the oscillation start voltage. However, it cannot lower the consumption current under the low power source voltage conditions.

An object of the present invention is to provide an oscillation circuit which exhibits low consumption current under a low power source voltage and has characteristics of both short oscillation start time and low oscillation start voltage.

According to one aspect of the present invention, there is provided an oscillation circuit comprising an oscillator composed of a quartz oscillator or a ceramic oscillator; a plurality of clocked inverters having the same circuit threshold values and controlled such that all clocked inverters begin their operations simultaneously at an oscillation start time and terminate their operations at mutually different times, inputs and outputs of which being connected in parallel across said oscillator; a control circuit for controlling said plurality of clocked invert-

ers; and an inverter having a constant-current means connected in series with the power source, and having its input and output being connected across said oscillator.

According to another aspect of the invention, there is provided an oscillation circuit comprising an oscillator composed of a quartz oscillator or a ceramic oscillator; a plurality of clocked inverters having the same circuit threshold values, inputs and outputs of which being connected in parallel across said oscillator; a control circuit generating control signals for said plurality of clocked inverters such that all clocked inverters begin their operations simultaneously at an oscillation start time and terminate their operations at mutually different times; an inverter having the same circuit threshold value as said plurality of clocked inverters, the input and output of which are short-circuited; and a voltage comparator driven by a constant current source, having a non-inverting input terminal, an inverting input terminal and an output terminal, said non-inverting input terminal being connected to said output of said inverter, said inverting input terminal being connected to said inputs of said plurality of clocked inverters, and said output terminal being connected to said outputs of said plurality of said clocked inverters.

According to a further aspect of the invention, there is provided an oscillation circuit comprising: an oscillator composed of a quartz oscillator or a ceramic oscillator; a plurality of clocked inverters having the same circuit threshold values and a control circuit generating control signals such that all clocked inverters begin their operations simultaneously at an oscillation start time and terminate their operations at mutually different times, inputs and outputs of all clocked inverters being connected in parallel across said oscillator; an inverter having the same circuit threshold value as said plurality of clocked inverters, an input and an output of which being short-circuited; and a linear amplifier circuit having a non-inverting input terminal, an inverting input terminal and an output terminal, said non-inverting input terminal being connected to said output of said inverter, said inverting input terminal being connected to said inputs of said plurality of clocked inverters, and said output terminal being connected to said outputs of said plurality of clocked inverters.

This invention can be more fully understood from the following detailed description when taken in conjunction with the accompanying drawings, in which:

Fig. 1 is a circuit diagram of a conventional oscillation circuit;
Fig. 2 is a circuit diagram of another conventional oscillation circuit;
Fig. 3 is a circuit diagram of a CMOS inverter in Figs. 1 and 2;
Fig. 4 is a circuit diagram of a first embodiment of an oscillation circuit according to the present invention;
Fig. 5 is a circuit diagram of the constant-current sources in the first embodiment in Fig. 4;
Fig. 6 is a circuit diagram of an example of the bias voltage generating circuit used in the circuit in Fig. 5;
Fig. 7 is a circuit diagram of an arrangement of the control circuit in the first embodiment in Fig. 4;
Fig. 8 is a circuit diagram of a detailed arrangement of the power-on clear circuit in Fig. 7;
Fig. 9 is a diagram for illustrating operation waveforms in the first embodiment in Fig. 4;
Figs. 10A to 10C are diagrams each showing current driving capability of the oscillation circuit in Fig. 4;
Figs. 11A and 11B are circuit diagrams of another arrangement of the inverter in Fig. 4;
Figs. 12A and 12B are circuit diagrams of still another arrangement of the inverter in Fig. 4;
Fig. 13 is a circuit diagram of a second embodiment of an oscillation circuit according to the present invention when taken together;
Fig. 14 is a circuit diagram of an arrangement of the voltage comparator in Fig. 13;
Fig. 15 is a circuit diagram of another arrangement of the voltage comparator in Fig. 13;
Fig. 16 is a circuit diagram of still another arrangement of the voltage comparator in Fig. 13;
Fig. 17 is a circuit diagram of a part of a third embodiment of an oscillation circuit according to the present invention; and
Fig. 18 is a circuit diagram of the inverter to be used in Fig. 13.

There will now be described in detail embodiments of an oscillation circuit according to the present invention with reference to the drawings.

Fig. 4 is a circuit diagram showing an arrangement of a first embodiment of the oscillation circuit according to the present invention. In Fig. 4, five CMOS clocked inverters 12 to 16, for example, and a feedback resistor 17 are connected in parallel across an oscillator 11 composed of a quartz oscillator or a ceramic oscillator. Control signal pairs $\phi 1$, $\overline{\phi 1}$; $\phi 2$, $\overline{\phi 2}$; $\phi 3$, $\overline{\phi 3}$; $\phi 4$, $\overline{\phi 4}$; and $\phi 5$, $\overline{\phi 5}$ are supplied to clock signal input terminals of the five CMOS clocked inverters 12 to 16, respectively. Operations of these clocked inverters 12 to 16 are controlled by corresponding control signal pairs. A capacitor 18 is connected between one terminal of the oscillator 11 and ground voltage Vss and a capacitor 19 is also connected between the other terminal of the oscillator 11 and ground voltage Vss. An input terminal and an output terminal of a CMOS inverter 20 is connected in parallel with the five clocked inverters 12 to 16 across the oscillator 11.

As shown in Fig. 4, the inverter 20 comprises a P-channel MOS transistor 21, the source and drain connections of which are inserted between the power source voltage Vcc and an output terminal, and the gate

of which is connected to the input terminal; an constant-current source 22 connected between the source of the MOS transistor 21 and the power source voltage Vcc and having a current value IP; an N-channel MOS transistor 23, the source and drain connections of which are connected between the output terminal and ground voltage Vss, and the gate of which is connected to the input terminal; and a constant-current source 24 connected between the source of the MOS transistor 23 and ground voltage Vss and having a current value IN. The current flowing through the inverter 20, i.e., current values IP and IN of the constant-current sources 22 and 24, is set in advance at the minimum value required to maintain the oscillation.

A control circuit 40 in Fig. 4 generates the control signal pairs $\phi 1$, $\overline{\phi 1}$; $\phi 2$, $\overline{\phi 2}$; $\phi 3$, $\overline{\phi 3}$; $\phi 4$, $\overline{\phi 4}$; and $\phi 5$, $\overline{\phi 5}$ which are used for the clocked inverters 12 to 16. The control circuit 40 energizes all the control signal pairs to operate the clocked inverters 12 to 16 at the start of oscillation. After a predetermined time has elapsed from the start of the oscillation, the control circuit 40 deenergizes the control signal pairs so that each control signal pair has an operation terminating time different from that of the others.

An inverter 29 is provided as a waveform shaping means for an output of the inverter 20. Since the output waveform of the inverter 20 does not fully swing between ground voltage Vss and power source voltage Vcc, the penetration current is increased sometimes if the output of the inverter 20 is used as an input signal of an ordinary inverter which is composed of a P-channel MOS transistor and an N-channel MOS transistor. However, if the output of the inverter 20 is waveform-shaped by the inverter 29 which has the same arrangement as the inverter 20, the penetration current can be controlled with the constant-current source and thus low consumption can be obtained. Since the inverter 29 has the same arrangement as the inverter 20, as shown in Fig. 4, a circuit threshold value of the inverter 29 is identical to that of the inverter 20. As a result, when an amplitude of the output of the inverter 20 is small, a waveform-shaped output can be produced from the inverter 29.

Fig. 5 is a circuit diagram of the constant-current sources 22 and 24 in the inverter 20 in the first embodiment of Fig. 4. The constant-current sources 22 and 24 comprise respectively a P-channel MOS transistor 25 a gate of which is supplied with a predetermined bias voltage V_{BiasP}; an N-channel MOS transistor 26 a gate of which is supplied with a predetermined bias voltage V_{BiasN}; and a bias voltage generating circuit 28 for generating the bias voltages V_{BiasP} and V_{BiasN}.

Fig. 6 is a circuit diagram of an example of the bias voltage generating circuit 28 used in the circuit of Fig. 5. In the generating circuit 28, a resistor 32 is connected to an emitter of an NPN bipolar transistor. Thus a predetermined collector current is caused to flow through the bipolar transistor 31 and therefore a substantially constant voltage, for example, almost 0.7V is generated between the base and the emitter of the bipolar transistor 31. This constant voltage is used to generate the bias voltages V_{BiasP} and V_{BiasN}. More particularly, a base-emitter voltage of the bipolar transistor 31 is applied across a resistor 33. A current flowing through the resistor 33 is supplied to a current-mirror circuit 34 as an input current. An output current of the current-mirror circuit 34 is also supplied to another current mirror circuit 35 as an input current. Further, an output current of the current-mirror circuit 35 is fed back to the current-mirror circuit 34 as an input current. The bias voltage V_{BiasN} which is applied to the gate of the N-channel MOS transistor 26 can be obtained as a voltage of a common node 36 between the current-mirror circuits 38 and 39. The bias voltage V_{BiasP} which is applied to the gate of the P-channel MOS transistor 25 can also be obtained by shifting the bias V_{BiasN} to the power source voltage Vcc side by an inverter 37.

Fig. 7 is a circuit diagram of an arrangement of the control circuit 40 in the embodiment of Fig. 4. The control circuit 40 comprises a power-on clear circuit 41 which generates a power-on clear signal with a predetermined pulse width when the power source is turned on; an up counter 42 which is reset by the power-on clear signal and to which a signal generated by the oscillation circuit including the control circuit 40 is supplied as a counter clock input CLK; four flip-flop circuits 43, 44, 45 and 46 which are commonly set by the power-on clear signal and are respectively reset by count output signals Q1, Q2, Q3 and Q4 of the up counter 42; and an inverter 47 for inverting the power-on clear signal. The control signals $\phi 1$ and $\overline{\phi 1}$ are outputted from the power-on clear circuit 41 and the inverter 47, respectively. The control signals $\phi 2$ and $\overline{\phi 2}$ are outputted from the flip-flop circuit 43, the control signals $\phi 3$ and $\overline{\phi 3}$ are outputted from the flip-flop circuit 44, the control signals $\phi 4$ and $\overline{\phi 4}$ are outputted from the flip-flop circuit 45, and the control signals $\phi 5$ and $\overline{\phi 5}$ are outputted from the flip-flop circuit 46.

Fig. 8 is a circuit diagram of a detailed arrangement of the power-on clear circuit 41 in Fig. 7. The circuit 41 comprises a voltage comparator 51 which has an inverting input terminal (-) and a non-inverting input terminal (+); a voltage divider circuit 52 which has two resistors connected serially between the power source voltage Vcc and the earth voltages Vss and divides the voltage Vcc at a predetermined ratio; and an integration circuit 53 which consists of a resistor and a capacitor connected serially between the power source voltage Vcc and the earth voltage Vss and integrates the voltage Vcc at a constant time constant when the power source is turned on. An output of the integration circuit 53 and an output of the voltage divider circuit 52 are inputted into the inverting input terminal (-) and the non-inverting input terminal (+) of the voltage comparator 51, respectively.

Operations of the first embodiment of the oscillation circuit shown in Fig. 4 will now be described with refer-

ence to Fig. 9. First, when the power source Vcc is turned on (Fig. 9(A)), the power-on clear signal with a predetermined pulse width and at an "H" level is generated by the power-on clear circuit 41 in the control circuit 40 of Fig. 7 (Fig. 9(B)). Thus the signals $\phi 1$ and $\overline{\phi 1}$ set at "H" and "L" levels at a time t_1, respectively, to energize the control signal pair $\phi 1$ and $\overline{\phi 1}$ (Fig. 9(B)). Then, four flip-flop circuits 43 to 46 are set by the power-on clear signal, respectively. As a result, the signals $\phi 2$, $\phi 3$, $\phi 4$ and $\phi 5$ are set simultaneously at an "H" level at the time t_1 (Fig. 9(C)(D)(E)(F)) whereas the signals $\overline{\phi 2}$, $\overline{\phi 3}$, $\overline{\phi 4}$, and $\overline{\phi 5}$ are set simultaneously at an "L" level. Therefore, the control signal pairs $\phi 2$, $\overline{\phi 2}$; $\phi 3$, $\overline{\phi 3}$; $\phi 4$, $\overline{\phi 4}$; and $\phi 5$, $\overline{\phi 5}$ are energized parallelly at the same time. During the time period t_1-t_2 in Fig. 9, all the clocked inverters 12 to 16 in Fig. 4 are operated. More particularly, all the clocked inverters 12 to 16 and the inverter 20 operate immediately after the turning-on of the power source, and, since the load is driven by a large amount of current, a time period required for beginning the oscillation is shortened. In the present invention, a beginning of the oscillation is defined such that an amplitude and a frequency of the oscillation output have predetermined values, respectively.

When the oscillation operation is stabilized to a certain extent after starting the oscillation (Fig. 9(G)), the output of the power-on clear circuit 41 is inverted at an "L" level at a time t_2 (Fig. 9(B)). A time period t_1-t_2 during when the output signal is inverted from an "H" level to an "L" level is determined beforehand by the time constant of the integration circuit 43 shown in Fig. 8. When the output of the power-on clear circuit 41 is inverted to an "L" level, the output of the inverter 47 in Fig. 7 is turned to an "H" level to deenergize the control signal pair $\phi 1$ and $\overline{\phi 1}$ (Fig. 9(B)). Hence, the clocked inverter 12 in operation stops its operation at the time t_2 and thus the output terminal becomes a high impedance state. The current driving capability for the load is decreased by the amount of the clocked inverter 12.

Following that the output of the power-on clear circuit 41 is changed to an "L" level, a reset of the up counter 42 in Fig. 7 and a set of four flip-flop circuits 43 to 46 are released. The up counter 42 thereafter starts to count the oscillation signals generated.

When a predetermined time t_2-t_3 elapsed from when the up counter 42 begins to count, a lower output signal Q1 is first raised to an "H" level (Fig. 9(H)). As a result, the flip-flop circuit 43 is reset to deenergize the control signal pair $\phi 2$, $\overline{\phi 2}$ which are the Q, $\overline{Q}$ output signals. Hence, the clocked inverter 13 in operation stops its operation and thus the current driving capability is further decreased by the amount of the clocked inverter 12. When the up counter 42 keeps the counts continuously, more significant output signals are raised sequentially to an "H" level at times t4, t5, and t6. The flip-flop circuits 44 to 46 are therefore reset in sequence and thus the clocked inverters 14 to 16 stop their operations successively (Figs. 9(I)(J) and (K)).

If all the clocked inverters 12 to 16 are set to have the same current driving capability, then total current driving capability is decreased by a constant amount, as shown in Fig. 10A, each time when one of the clocked inverters 12 to 16 stops its operation. That is, the current driving capability of all the inverters can be changed linearly. The abscissa of Fig. 10A is a time axis.

As described above, the operations of a plurality of clocked inverters are stopped sequentially one by one so that all the current driving capability including that of the inverter 20 are sequentially decreased. Hence, the disadvantage such that the oscillation has to be stopped in the course of the operation does not occur.

After the clocked inverters stop perfectly, a feedback circuit is formed by the inverter 20 alone. A minimum current required to maintain the oscillation can be flown through the inverter 20. A constant current can always be passed through the inverter 20 even if the variations of the power source voltage Vcc and the threshold voltages of the transistors 21 and 23 are caused. The consumption current can therefore be lowered in a stationary state where the oscillation operation is stable.

In the above embodiment, five clocked inverters 12 to 16 each has the same current driving capability are used. However, in such case, the stable oscillation operation is wrongly affected with the marked variation of the current driving capability due to the turn off of the last clocked inverter 16. Hence, as another modification, the current driving capabilities of five clocked inverters 12 to 16 can be reduced gradually by 1/2, for example, with respect to that of the previous clocked inverter. This is shown in Fig. 10B. In this modification, the current driving capability is changed nonlinearly. More particularly, all the clocked inverters is operating during the time period t_1-t_2. At the time t2 when the clocked inverter 12 is caused to stop, the current driving capability of all the clocked inverters is reduced to half of that obtained at the time t1. At the time t3 when the clocked inverter 13 is caused to stop, the current driving capability of all the clocked inverters is further reduced to half of that obtained at the time t2. Like this, a bad influence upon the stable oscillation operation, which is caused by the turn off of the clocked inverter, can be suppressed by lowering the current driving capability of all the clocked inverters by 50%, for example, every turn off of the clocked inverter. At that time, the current driving capability of all the clocked inverters is not necessarily reduced by 50%. Namely, the current drive ability may be changed nonlinearly, as shown in Fig. 10B.

Moreover, as shown in Fig. 10C, it is possible that the operation of the last clocked inverter 16 is not stopped when the oscillation circuit is in oscillation operation.

Furthermore, in the first embodiment, constant-current sources are provided in both P-channel and N-channel transistor sides. However, as shown in Figs. 11A and 11B, the constant-current source may be provided only in the P-channel transistor side and also, as

shown in Figs. 12A and 12B, the constant-current source may also be provided only in the N-channel transistor side.

Next, a second embodiment of the oscillation circuit according to the present invention will be described with reference to Fig. 13.

In the second embodiment, a circuit consisting of a CMOS inverter 61 and a voltage comparator 62 is used instead of the CMOC inverter 20 in which constant-current sources are connected between the power source voltage Vcc and the earth voltage Vss. Since the arrangement of the second embodiment except for the above circuit are identical to those of the circuit of Fig. 4, the descriptions thereof are omitted. The inverter 61 has the same threshold voltage as those of five clocked inverters 12 to 16. An input terminal and an output terminal of the inverter 61 are connected each other to short-circuit. Accordingly the inverter 61 generates an output voltage which is equivalent to a threshold value of the circuit. The output terminal of the inverter 61 is connected to a non-inverting input terminal (+) of the CMOS voltages comparator 62 using P-channel and N-channel MOS transistors. A constant-current source which is controlled by the predetermined voltage V_{BiasN} is provided in the voltage comparator 62. The voltage V_{BiasN} is generated by the same circuit as in Fig. 6. The inverting input terminal (-) of the voltage comparator 62 is connected to input terminals of five clocked inverters 12 to 16 in parallel. The output terminal of the comparator 62 is also connected to output terminals of five clocked inverters 12 to 16 in parallel. The comparator 62 compares a voltages inputted into the non-inverting input terminal with a voltage inputted into the inverting input terminal. An input voltage to the non-inverting input terminal is used as a threshold voltage for an input voltage to the inverting input terminal. The circuit consisting of the inverter 61 and the voltage comparator 62 operates an inverter for inverting the input signal, like the inverter 20 in the circuit in Fig. 4. In the second embodiment, the circuit threshold voltage of the inverter 61 is designed to be equal to those of five clocked inverter 12 to 16. Hence, even when the circuit threshold voltage of the clocked inverters 12 to 16 and the power source voltage are varied, the circuit consisting of the inverter 61 and the voltage comparator 62 is also affected by the above variations. As a result, when the variations in the circuit threshold voltage and the power source voltage occur, an operating point of the oscillation of the voltage comparator 62 which operates as an inverter also changes according to the above variations of the clocked inverters 12 to 16 to thus suppress the influence to the above variations.

Fig. 14 is a circuit diagram of an arrangement of the voltage comparator 62 in Fig. 13. The voltage comparator 62 comprises a differential pair which is made of a pair of N-channel MOS transistors 71 and 72; a current mirror circuit which is made of a pair of P-channel transistors 73 and 74 and operates as a load of the differential pair; a constant-current source made of N-channel MOS transistor 75; a P-channel MOS transistor 76 which receives an output from the differential pair; and a constant-current source made of N-channel MOS transistor 77. Sources of the transistors 71 and 72 are commonly connected. Drains of the transistors 73 and 74 are connected to drains of the transistors 71 and 72 respectively and gates thereof are commonly connected to a drain of the transistor 71. The bias voltage V_{BiasN} is supplied to a gate of the transistor 75 which provides the differential pair with a predetermined operating current. The transistor 77 is serially connected to the output transistor 76. The bias voltage V_{BiasN} is supplied to a gate of the transistor 77. The transistor 77 supplies a predetermined operating current to the output transistor 76.

With the above voltage comparator 62, a current flowing through the voltage comparator 62 may be limited by N-channel MOS transistors 75 and 77 of the constant-current source when only the circuit consisting of the inverter 61 and the voltage comparator 62 operates as the feedback circuit after all the clocked inverters 12 to 16 are turned off. Hence, a low consumption current may be attained in the oscillation circuit. A current is also consumed in the inverter 61. However, the inverter 61 may merely output a voltage equal to the circuit threshold voltage which is determined by a driving ratio of the P-channel side and the N-channel side of the oscillation circuit. Therefore, if a certain constant ratio is kept and gate lengths of both transistors are lengthened, a penetration current may be decreased sufficiently even taking the variations into consideration. Consequently, an increase in total consumption current is very little.

Fig. 15 is a circuit diagram of another arrangement of the voltage comparator 62 in Fig. 13. In this voltage comparator 62, a resistor 78 is inserted between a drain of the N-channel MOS transistor 72 which is a part of the differential pair and a common gate of a pair of P-channel MOS transistors 73 and 74 which comprises the current mirror circuit. A voltage amplification factor of the comparator 62 is lowered by the resistor 78. Thus an output waveform are not rectangular waveform due to the saturation of the voltage.

Fig. 16 is a circuit diagram of still another arrangement of the voltage comparator 62 in Fig. 13. As shown in Fig. 15, in case the voltage amplification factor of the voltage comparator is still high even when the resistor 78 is inserted between the common gate of the transistor 73 and 74 and the drain of the transistor 72, only the preceding differential pairs are used as a feedback circuit, but the succeeding inverter consisting of the P-channel MOS transistor 76, i.e., output transistor and the N-channel MOS transistor 77, i.e., constant-current source is used as a waveform shaping inverter.

As shown in Fig. 10B, the current driving capability of the clocked inverter can be set at half, for example, in contrast to that of the preceding clocked inverter, instead of setting the current driving capability of five

clocked inverts 12 to 16 to be the same. Further, as shown in Fig. 10C, the last clocked inverter 16 is able to continue to operate.

As shown in Fig. 17, instead of the voltage comparator in the second embodiment, a CMOS linear amplifier circuit 91 can be used. The resistors 92 and 93 are provided as gain adjusting resistors.

In the embodiment of Fig. 13, the inverter 61 is used. However, the clocked inverter can be used so as to coincide the circuit threshold voltage with the threshold voltages of the clocked inverters 12 to 16, instead of the inverter 61. More particularly, since the clocked inverter is operated as the ordinary inverter in such case, the earth voltage VSS is supplied to one of two P-channel MOS transistors 95 and 96 whereas the power source voltages Vcc is supplied to one of two N-channel MOS transistors 97 and 98, as shown in Fig. 18.

As described above, the comparator having a low gain characteristic (Fig. 15) and the linear amplifier (Fig. 17) can be used in the second embodiment instead of the comparator 62 in Fig. 13. When the output signal of such comparator and such linear amplifier is waveform-shaped, the oscillation waveform of small amplitude can be surely amplified if the same arrangement circuit as such comparator and such linear amplifier is used as the waveform shaping means. In such case, the consumption current can also be controlled, as in the first embodiment in Fig. 4.

As disclosed in the above,since the clocked inverter operates during a predetermined period of time after the start of the oscillation, a feedback circuit is formed by both the clocked inverter and the inverter at the start time of the oscillation. The oscillation circuit is therefore driven by a large current and thus the oscillation start time can be shorten and also the oscillation start voltage can be lowered. On the other hand, the oscillation circuit is driven only by the inverter after starting the oscillation. Since a constant current means is inserted serially in the path of the power source of the inverter, the constant operating current always flows through the inverter without being affected by the variations of the threshold voltage of the transistors and the variations of the power source voltages. As a result, a low consumption current characteristic of the oscillation circuit can be obtained.

Claims

1. An oscillation circuit comprising:

   an oscillator (11) composed of a quartz oscillator or a ceramic oscillator;
   a plurality of clocked inverters (12, 13, 14, 15, 16) having the same circuit threshold values, inputs and outputs of which being connected in parallel across said oscillator (11);
   a control circuit (40) generating control signals for said plurality of clocked inverters (12, 13, 14, 15, 16) such that all clocked inverters (12, 13, 14, 15, 16) begin their operations simultaneously at an oscillation start time and terminate their operations at mutually different times; and
   an inverter (20) having a constant-current means (22, 24) connected in series with the power source, and having its input and output being connected across said oscillator (11).

2. An oscillation circuit according to claim 1, wherein said plurality of clocked inverters (12, 13, 14, 15, 16) have the same output driving capabilities with each other.

3. An oscillation circuit according to claim 1, wherein current driving capabilities of said plurality of clocked inverters (12, 13, 14, 15, 16) are set such that a total output drive current of said plurality of clocked inverters (12, 13, 14, 15, 16) is changed nonlinearly when operations of said plurality of clocked inverters (12, 13, 14, 15, 16) are sequentially terminated.

4. An oscillation circuit according to claim 3, wherein the clocked inverter (16) having the smallest output drive current value is controlled to operate continuously from the oscillation start time to the oscillation termination time.

5. An oscillation circuit comprising:

   an oscillator (11) composed of a quartz oscillator or a ceramic oscillator;
   a plurality of clocked inverters (12, 13, 14, 15, 16) having the same circuit threshold values, inputs and outputs of which being connected in parallel across said oscillator (11);
   a control circuit (40) generating control signals for said plurality of clocked inverters (12, 13, 14, 15, 16) such that all clocked inverters (12, 13, 14, 15, 16) begin their operations simultaneously at an oscillation start time and terminate their operations at mutually different times;
   an inverter (61) having the same circuit threshold value as said plurality of clocked inverters (12, 13, 14, 15, 16), the input and output of which are short-circuited; and
   a voltage comparator (62) driven by a constant current source, having a non-inverting input terminal, an inverting input terminal and an output terminal, said non-inverting input terminal being connected to said output of said inverter (61), said inverting input terminal being connected to said inputs of said plurality of clocked inverters (12, 13, 14, 15, 16), and said output terminal being connected to said outputs of said plurality of said clocked inverters (12, 13, 14, 15, 16).

6. An oscillation circuit according to claim 5, wherein said plurality of clocked inverters (12, 13, 14, 15, 16) have the same output driving capabilities as each other.

7. An oscillation circuit according to claim 5, wherein current driving capabilities of said plurality of clocked inverters (12, 13, 14, 15, 16) are set such that the total output drive current of said plurality of clocked inverters (12, 13, 14, 15, 16) is changed nonlinearly when operations of said plurality of clocked inverters (12, 13, 14, 15, 16) are sequentially terminated.

8. An oscillation circuit according to claim 7, wherein the clocked inverter (16) having a smallest output drive current value is controlled to operate continuously throughout from the oscillation start time to the oscillation termination time.

9. An oscillation circuit according to claim 6, wherein said voltage comparator (62) comprises:

a differential pair (71, 72) composed of a first and a second transistor of a first conductivity, gates of which being connected to said one input terminal and said the other input terminal respectively and sources of which being connected commonly;
a third transistor (73) of a second conductivity, a source-drain connection of which is connected between a power source of a high electric potential side and said drain of said first transistor and a drain and a gate of which are commonly connected;
a fourth transistor (74) of a second conductivity, a source-drain connection of which is connected between said power source of said high electric potential side and said drain of said second transistor and said gate of which is connected to said gate of said third transistor;
a fifth transistor (75) of a first conductivity, a source-drain connection of which is connected between a power source of a low electric potential and a source common connecting point of said first and said second transistor and a gate of which is supplied by a predetermined bias voltage; and
a resistor (78) connected between said drain of said second transistor and a gate common connecting point of said third and fourth transistors.

10. An oscillation circuit according to claim 5, wherein said inverter (61) has the same circuit as each of said plurality of clocked inverters (12, 13, 14, 15, 16).

11. An oscillation circuit comprising:

an oscillator (11) composed of a quartz oscillator or a ceramic oscillator;
a plurality of clocked inverters (12, 13, 14, 15, 16) having the same circuit threshold values, inputs and outputs of which being connected in parallel across said oscillator (11);
a control circuit (40) generating control signals for said plurality of clocked inverters (12, 13, 14, 15, 16) such that all clocked inverters (12, 13, 14, 15, 16) begin their operations simultaneously at an oscillation start time and terminate their operations at mutually different times;
an inverter (61) having the same circuit threshold value as said plurality of clocked inverters (12, 13, 14, 15, 16), an input and an output of which being short-circuited; and
a linear amplifier circuit (91, 92, 93) having a non-inverting input terminal, an inverting input terminal and an output terminal, said non-inverting input terminal being connected to said output of said inverter (61), said inverting input terminal being connected to said inputs of said plurality of clocked inverters (12, 13, 14, 15, 16), and said output terminal being connected to said outputs of said plurality of clocked inverters (12, 13, 14, 15, 16).

Patentansprüche

1. Oszillations-Schaltkreis, der folgendes aufweist:

einen Oszillator (11), der aus einem Quarzoszillator oder einem Keramikoszillator gebildet ist;
eine Vielzahl getakteter Inverter (12, 13, 14, 15, 16) mit denselben Schaltkreis-Schwellenwerten, deren Eingänge und Ausgänge über den Oszillator (11) parallel geschaltet sind;
eine Steuerschaltung (40), die Steuersignale für die Vielzahl getakteter Inverter (12, 13, 14, 15, 16) erzeugt, so daß alle getakteten Inverter (12, 13, 14, 15, 16) ihre Operationen zu einer Oszillations-Startzeit gleichzeitig beginnen und ihre Operationen zu zueinander unterschiedlichen Zeiten beenden; und
einen Inverter (20) mit einer Konstantstromeinrichtung (22, 24), die zur Leistungsversorgung in Reihe geschaltet ist, und dessen Eingang und Ausgang über den Oszillator (11) angeschlossen ist.

2. Oszillations-Schaltkreis nach Anspruch 1, wobei die Vielzahl getakteter Inverter (12, 13, 14, 15, 16) dieselben Ausgangsantriebsfähigkeiten zueinander haben.

3. Oszillations-Schaltkreis nach Anspruch 1, wobei

Stromantriebsfähigkeiten der Vielzahl getakteter Inverter (12, 13, 14, 15, 16) derart eingestellt sind, daß ein gesamter ausgegebener Antriebsstrom der Vielzahl getakteter Inverter (12, 13, 14, 15, 16) nicht linear geändert wird, wenn Operationen der Vielzahl getakteter Inverter (12, 13, 14, 15, 16) aufeinanderfolgend beendet werden.

4. Oszillations-Schaltkreis nach Anspruch 3, wobei der getaktete Inverter (16) mit dem kleinsten ausgegebenen Antriebsstromwert gesteuert wird, um von der Oszillations-Startzeit bis zur Oszillations-Beendigungszeit kontinuierlich zu arbeiten.

5. Oszillations-Schaltkreis, der folgendes aufweist:

einen Oszillator (11), der aus einem Quarzoszillator oder einem Keramikoszillator gebildet ist;
eine Vielzahl getakteter Inverter (12, 13, 14, 15, 16) mit denselben Schaltkreis-Schwellenwerten, deren Eingänge und Ausgänge über den Oszillator (11) parallel geschaltet sind;
eine Steuerschaltung (40), die Steuersignale für die Vielzahl getakteter Inverter (12, 13, 14, 15, 16) erzeugt, so daß alle getakteten Inverter (12, 13, 14, 15, 16) ihre Operationen zu einer Oszillations-Startzeit gleichzeitig beginnen und ihre Operationen zu zueinander unterschiedlichen Zeiten beenden;
einen Inverter (61) mit demselben Schaltkreis-Schwellenwert wie die Vielzahl getakteter Inverter (12, 13, 14, 15, 16), dessen Eingang und Ausgang kurzgeschlossen sind; und
einen Spannungskomparator (62), der durch einen Konstantstromquelle betrieben wird, mit einem nicht invertierenden Eingangsanschluß, einem invertierenden Eingangsanschluß und einem Ausgangsanschluß, wobei der nicht invertierende Eingangsanschluß an den Ausgang des Inverters (61) angeschlossen ist, wobei der invertierende Eingangsanschluß an die Eingänge der Vielzahl getakteter Inverter (12, 13, 14, 15, 16) angeschlossen ist, und wobei der Ausgangsanschluß an die Ausgänge der Vielzahl der getakteten Inverter (12, 13, 14, 15, 16) angeschlossen ist.

6. Oszillations-Schaltkreis nach Anspruch 5, wobei die Vielzahl getakteter Inverter (12, 13, 14, 15, 16) dieselben Ausgangsantriebsfähigkeiten zueinander haben.

7. Oszillations-Schaltkreis nach Anspruch 5, wobei Stromantriebsfähigkeiten der Vielzahl getakteter Inverter (12, 13, 14, 15, 16) derart eingestellt sind, daß der gesamte Ausgangsantriebsstrom der Vielzahl getakteter Inverter (12, 13, 14, 15, 16) nicht linear geändert wird, wenn Operationen der Vielzahl getakteter Inverter (12, 13, 14, 15, 16) aufeinanderfolgend beendet werden.

8. Oszillations-Schaltkreis nach Anspruch 7, wobei der getaktete Inverter (16) mit einem kleinsten Ausgangsantriebsstromwert gesteuert wird, um ab der Oszillations-Startzeit bis zur Oszillations-Beendigungszeit kontinuierlich zu arbeiten.

9. Oszillations-Schaltkreis nach Anspruch 6, wobei der Spannungskomparator (62) folgendes aufweist:

ein Differenzierpaar (71, 72), das aus einem ersten und einem zweiten Transistor einer ersten Leitfähigkeit gebildet ist, deren Gate-Anschlüsse jeweils an den einen Eingangsanschluß und den anderen Eingangsanschluß angeschlossen sind und deren Source-Anschlüsse auf einen gemeinsamen Anschluß gelegt sind;
einen dritten Transistor (73) einer zweiten Leitfähigkeit, deren Source-Drain-Anschluß zwischen einer Leistungsversorgung einer Seite eines hohen elektrischen Potentials und dem Drain-Anschluß des ersten Transistors angeschlossen ist, und dessen Drain-Anschluß und Gate-Anschluß auf einen gemeinsamen Anschluß gelegt sind;
einen vierten Transistor (74) einer zweiten Leitfähigkeit, deren Source-Drain-Verbindung zwischen der Leistungsversorgung der Seite hohen elektrischen Potentials und dem Drain-Anschluß des zweiten Transistors angeschlossen ist, und dessen Gate-Anschluß an den Gate-Anschluß des dritten Transistors angeschlossen ist;
einen fünften Transistor (75) einer ersten Leitfähigkeit, dessen Source-Drain-Verbindung zwischen einer Leistungsversorgung eines niedrigen elektrischen Potentials und einer gemeinsamen Source-Verbindungsstelle des ersten und des zweiten Transistors angeschlossen ist, und dessen Gate-Anschluß durch eine vorbestimmte Vorspannung versorgt wird; und
einen Widerstand (78), der zwischen dem Drain-Anschluß des zweiten Transistors und einer gemeinsamen Gate-Verbindungsstelle des dritten und des vierten Transistors angeschlossen ist.

10. Oszillations-Schaltkreis nach Anspruch 5, wobei der Inverter (61) dieselbe Schaltung wie jeder der Vielzahl getakteter Inverter (12, 13, 14, 15, 16) hat.

11. Oszillations-Schaltkreis, der folgendes aufweist:

einen Oszillator (11), der aus einem Quarzos-

zillator oder einem Keramikoszillator gebildet ist;
eine Vielzahl getakteter Inverter (12, 13, 14, 15, 16) mit denselben Schaltkreis-Schwellenwerten, deren Eingänge und Ausgänge über den Oszillator (11) parallel geschaltet sind;
eine Steuerschaltung (40), die Steuersignale für die Vielzahl getakteter Inverter (12, 13, 14, 15, 16) erzeugt, so daß alle getakteten Inverter (12, 13, 14, 15, 16) ihre Operationen zu einer Oszillations-Startzeit gleichzeitig beginnen und ihre Operationen zu zueinander unterschiedlichen Zeiten beenden;
einen Inverter (61) mit demselben Schaltkreis-Schwellenwert wie die Vielzahl getakteter Inverter (12, 13, 14, 15, 16), von welchem ein Eingang und ein Ausgang kurzgeschlossen sind; und
eine lineare Verstärkerschaltung (91, 92, 93) mit einem nicht invertierenden Eingangsanschluß, einem invertierenden Eingangsanschluß und einem Ausgangsanschluß, wobei der nicht invertierende Eingangsanschluß an den Ausgang des Inverters (61) angeschlossen ist, wobei der invertierende Eingangsanschluß an die Eingänge der Vielzahl getakteter Inverter (12, 13, 14, 15, 16) angeschlossen ist, und wobei der Ausgangsanschluß an die Ausgänge der Vielzahl getakteter Inverter (12, 13, 14, 15, 16) angeschlossen ist.

Revendications

1. Un circuit oscillateur comprenant :

   un oscillateur (11) constitué par un oscillateur à quartz ou un oscillateur à céramique;
   un ensemble d'inverseurs synchrones (12, 13, 14, 15, 16) ayant les mêmes valeurs de seuil de circuit, dont les entrées et les sorties sont connectées en parallèle aux bornes de l'oscillateur (11);
   un circuit de commande (40) qui génère des signaux de commande pour l'ensemble d'inverseurs synchrones (12, 13, 14, 15, 16), de façon que tous les inverseurs synchrones (12, 13, 14, 15, 16) commencent à fonctionner simultanément à un instant de démarrage d'oscillation et cessent de fonctionner à des instants mutuellement différents; et
   un inverseur (20) ayant des moyens à courant constant (22, 24) connectés en série avec la source d'alimentation, et ayant son entrée et sa sortie connectées aux bornes de l'oscillateur (11).

2. Un circuit oscillateur selon la revendication 1, dans lequel l'ensemble d'inverseurs synchrones (12, 13, 14, 15, 16) ont mutuellement les mêmes capacité d'attaque de sortie.

3. Un circuit oscillateur selon la revendication 1, dans lequel les capacités d'attaque en courant de l'ensemble d'inverseurs synchrones (12, 13, 14, 15, 16) sont fixées de façon qu'un courant d'attaque de sortie total de l'ensemble des inverseurs synchrones (12, 13, 14, 15, 16) change de façon non linéaire au moment de l'arrêt séquentiel du fonctionnement de l'ensemble d'inverseurs synchrones (12, 13, 14, 15, 16).

4. Un circuit oscillateur selon la revendication 3, dans lequel l'inverseur synchrone (16) ayant la plus petite valeur de courant d'attaque de sortie est commandé de façon à fonctionner continuellement depuis l'instant de démarrage d'oscillation jusqu'à l'instant de fin d'oscillation.

5. Un circuit oscillateur comprenant :

   un oscillateur (11) constitué par un oscillateur à quartz ou un oscillateur à céramique;
   un ensemble d'inverseurs synchrones (12, 13, 14, 15, 16) ayant les mêmes valeurs de seuil de circuit, et dont les entrées et les sorties sont connectées en parallèle aux bornes de l'oscillateur (11);
   un circuit de commande (40) qui génère des signaux de commande pour l'ensemble d'inverseurs synchrones (12, 13, 14, 15, 16), de façon que tous les inverseurs synchrones (12, 13, 14, 15, 16) commencent à fonctionner simultanément à un instant de démarrage d'oscillation et cessent de fonctionner à des instants mutuellement différents;
   un inverseur (61) ayant la même valeur de seuil de circuit que l'ensemble d'inverseurs synchrones (12, 13, 14, 15, 16), dont l'entrée et la sortie sont court-circuitées; et
   un comparateur de tension (62), attaqué par une source de courant constant, ayant une borne d'entrée non inverseuse, une borne d'entrée inverseuse et une borne de sortie, la borne d'entrée non inverseuse étant connectée à la sortie de l'inverseur précité (61), la borne d'entrée inverseuse étant connectée aux entrées de l'ensemble d'inverseurs synchrones (12, 13, 14, 15, 16), et la borne de sortie étant connectée aux sorties de l'ensemble d'inverseurs synchrones (12, 13, 14, 15, 16).

6. Un circuit oscillateur selon la revendication 5, dans lequel l'ensemble d'inverseurs synchrones (12, 13, 14, 15, 16) ont mutuellement les mêmes capacité d'attaque de sortie.

7. Un circuit oscillateur selon la revendication 5, dans lequel les capacités d'attaque en courant de l'ensemble d'inverseurs synchrones (12, 13, 14, 15, 16) sont fixées de façon qu'un courant d'attaque de sortie total de l'ensemble des inverseurs synchrones (12, 13, 14, 15, 16) change de façon non linéaire au moment de l'arrêt séquentiel du fonctionnement de l'ensemble d'inverseurs synchrones (12, 13, 14, 15, 16).

8. Un circuit oscillateur selon la revendication 7, dans lequel l'inverseur synchrone (16) ayant la plus petite valeur de courant d'attaque de sortie est commandé de façon à fonctionner continuellement depuis l'instant de démarrage d'oscillation jusqu'à l'instant de fin d'oscillation.

9. Un circuit oscillateur selon la revendication 6, dans lequel le comparateur de tension (62) comprend :

une paire différentielle (71, 72) constituée par des premier et second transistors d'un premier type de conductivité dont les grilles sont respectivement connectées à la borne d'entrée précitée et à l'autre borne d'entrée, et dont les sources sont connectées en commun,
un troisième transistor (73) d'un second type de conductivité, dont une connexion source-drain est connectée entre une source d'alimentation d'un côté de potentiel électrique haut, et le drain du premier transistor, et dont un drain et une grille sont connectés en commun ;
un quatrième transistor (74) d'un second type de conductivité, dont une connexion source-drain est connectée entre la source d'alimentation du côté du potentiel électrique haut et le drain du second transistor, et dont la grille est connectée à la grille du troisième transistor; et
un cinquième transistor (75) d'un premier type de conductivité, dont une connexion source-drain est connectée entre une source d'alimentation d'un côté de potentiel électrique bas et un point de connexion commun des sources des premier et second transistors, et dont une grille reçoit une tension de polarisation prédéterminée; et
une résistance (78) connectée entre le drain du second transistor et un point de connexion commun aux grilles des troisième et quatrième transistors.

10. Un circuit oscillateur selon la revendication 5, dans lequel l'inverseur (61) a le même circuit que chacun des éléments de l'ensemble d'inverseurs synchrones (12, 13, 14, 15, 16).

11. Un circuit oscillateur comprenant :

un oscillateur (11) constitué par un oscillateur à quartz ou un oscillateur à céramique;
un ensemble d'inverseurs synchrones (12, 13, 14, 15, 16) ayant les mêmes valeurs de seuil de circuit, dont les entrées et les sorties sont connectées en parallèle aux bornes de l'oscillateur (11);
un circuit de commande (14) qui génère des signaux de commande pour l'ensemble d'inverseurs synchrones (12, 13, 14, 15, 16), de façon que tous les inverseurs synchrones (12, 13, 14, 15, 16) commencent à fonctionner simultanément à un instant de départ d'oscillation et cessent de fonctionner à des instants mutuellement différents;
un inverseur (61) ayant la même valeur de seuil de circuit que les éléments de l'ensemble d'inverseurs synchrones (12, 13, 14, 15, 16), dont l'entrée et la sortie sont court-circuitées; et
un circuit amplificateur linéaire (91, 92, 93) ayant une borne d'entrée non inverseuse, une borne d'entrée inverseuse et une borne de sortie, la borne d'entrée non inverseuse étant connectée à la sortie de l'inverseur (61), la borne d'entrée inverseuse étant connectée aux entrées de l'ensemble d'inverseurs synchrones (12, 13, 14, 15, 16), et la borne de sortie étant connectée aux sorties de l'ensemble d'inverseurs synchrones (12, 13, 14, 15, 16).

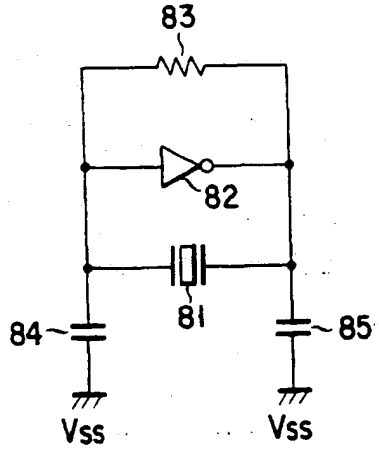


FIG. 1

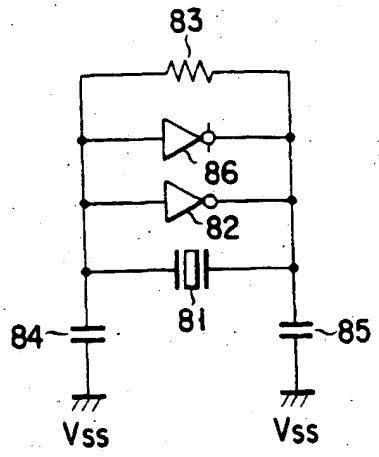


FIG. 2

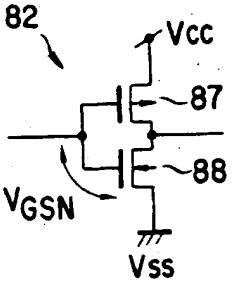


FIG. 3

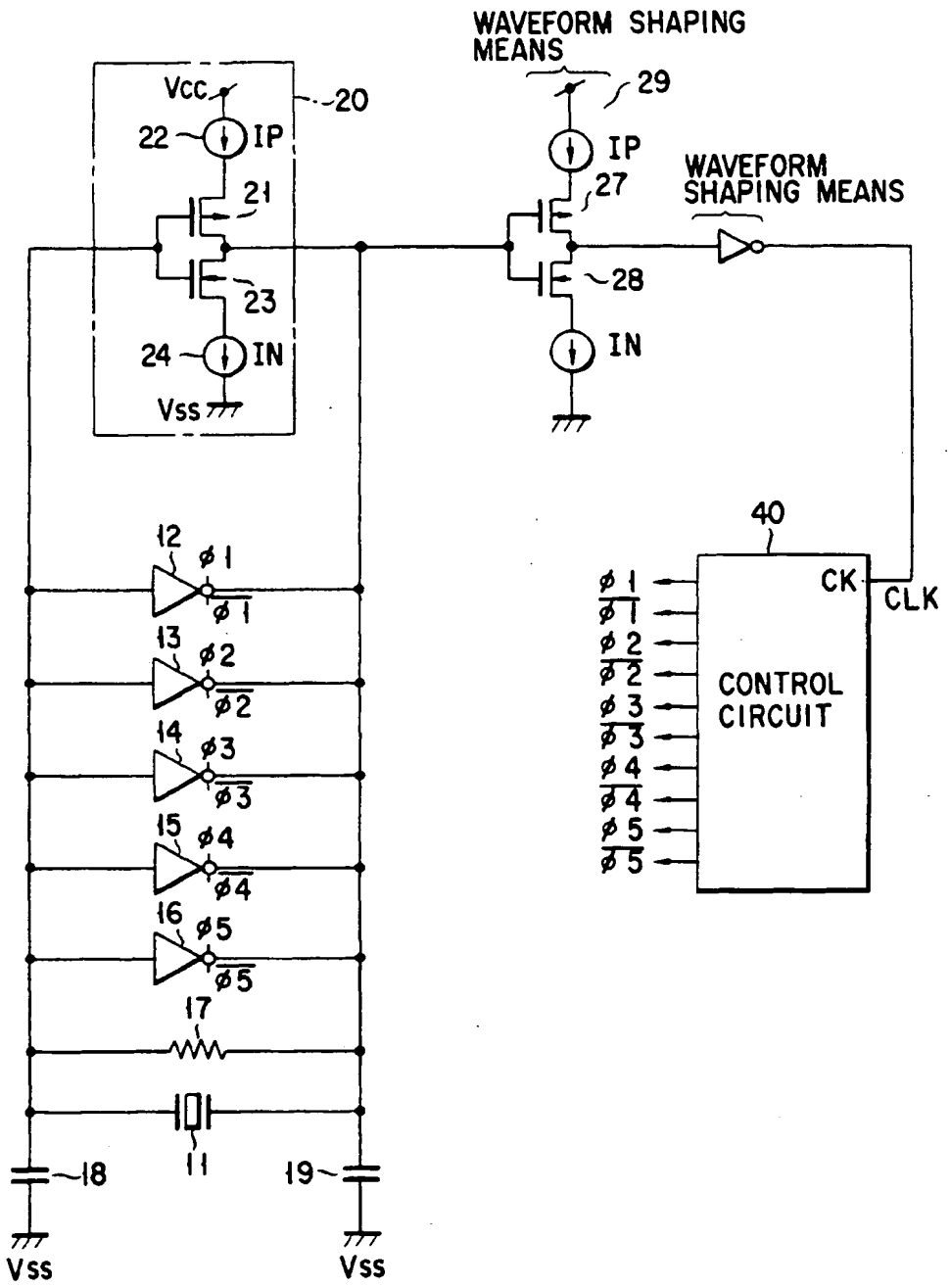

WAVEFORM SHAPING MEANS
Vcc
20
22
IP
21
23
24
IN
Vss
29
IP
27
28
IN
WAVEFORM SHAPING MEANS
40
CK
CLK
CONTROL CIRCUIT
12
13
14
15
16
17
18
11
19
Vss
Vss

FIG. 4

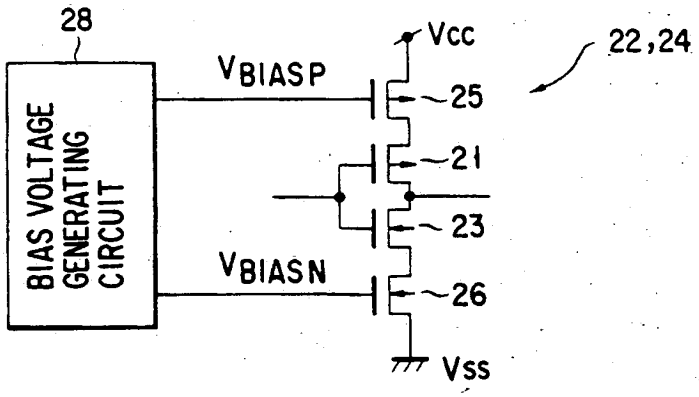

28
BIAS VOLTAGE GENERATING CIRCUIT
VBIASP
VBIASN
Vcc
Vss
22,24
25
21
23
26

FIG. 5

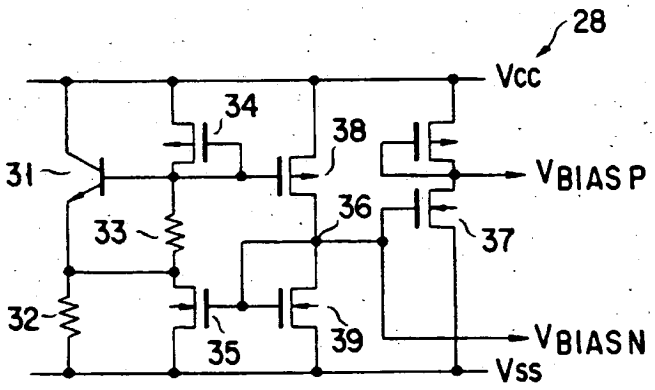

28
Vcc
34
38
31
VBIASP
36
33
37
32
35
39
VBIASN
Vss

FIG. 6

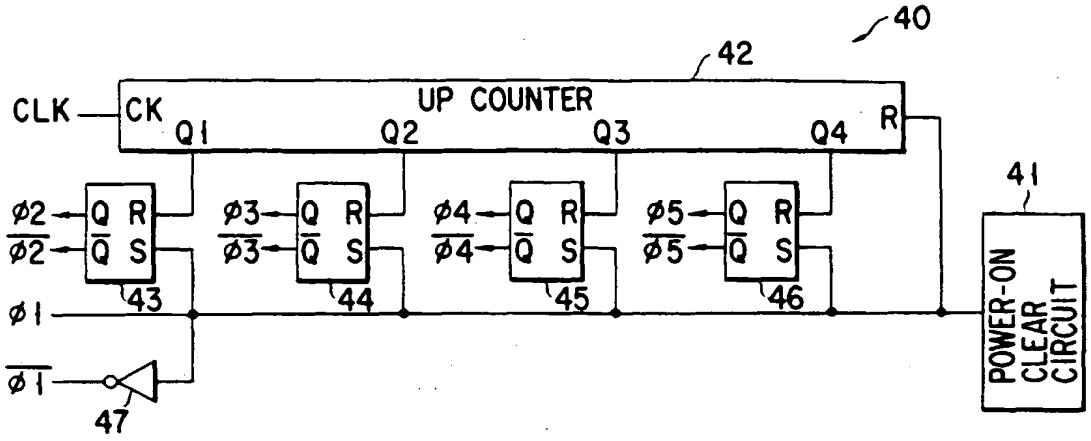

40
42
CLK
CK
UP COUNTER
Q1
Q2
Q3
Q4
R
41
ø2
ø2
ø3
ø3
ø4
ø4
ø5
ø5
Q
Q̄
R
S
43
44
45
46
ø1
ø1
47
POWER-ON
CLEAR
CIRCUIT

FIG. 7

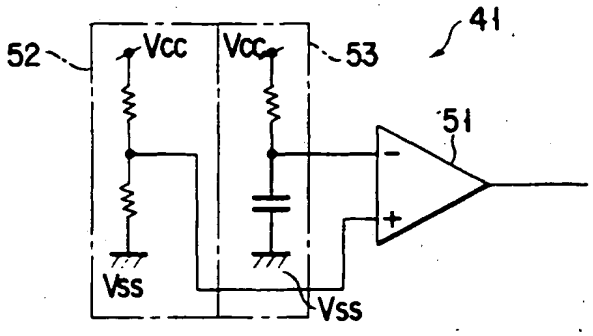

41
52
Vcc
Vcc
53
51
Vss
Vss

FIG. 8

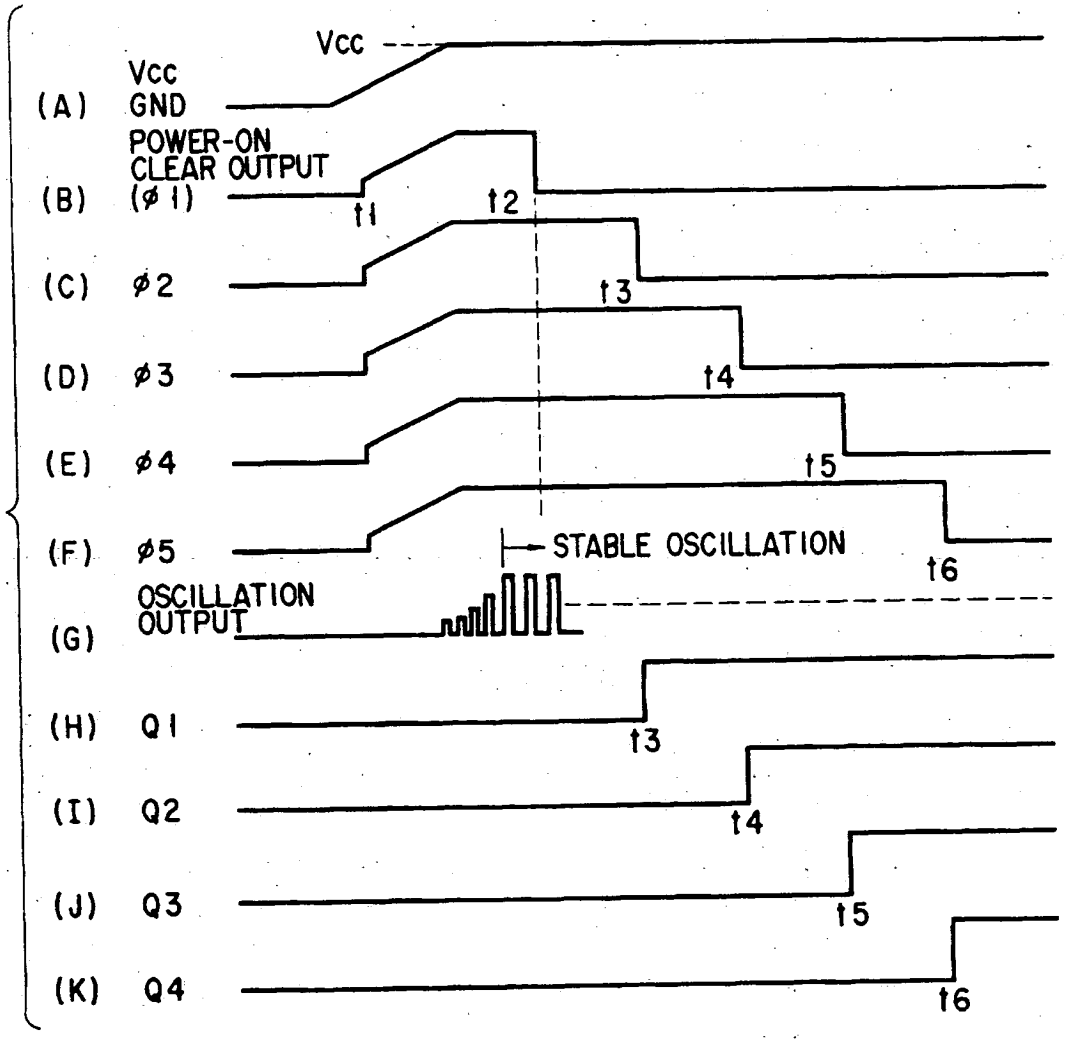

Vcc
(A) Vcc
GND
POWER-ON
CLEAR OUTPUT
(B) (ø1)
t1
t2
(C) ø2
t3
(D) ø3
t4
(E) ø4
t5
(F) ø5
STABLE OSCILLATION
t6
OSCILLATION
OUTPUT
(G)
(H) Q1
t3
(I) Q2
t4
(J) Q3
t5
(K) Q4
t6

FIG. 9

FIG. 10A

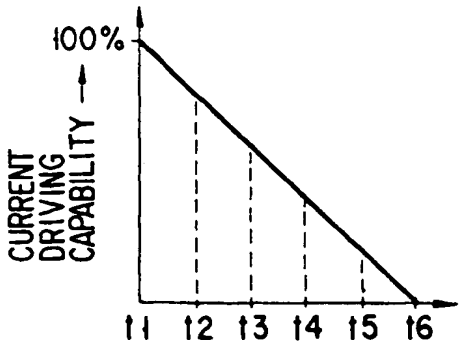


FIG. 10B

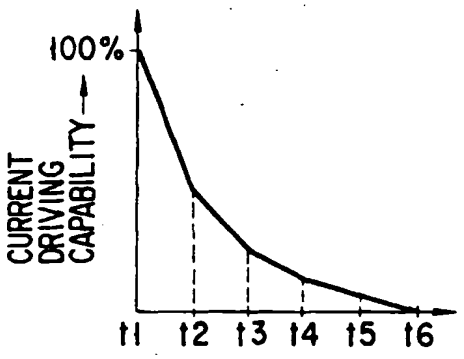
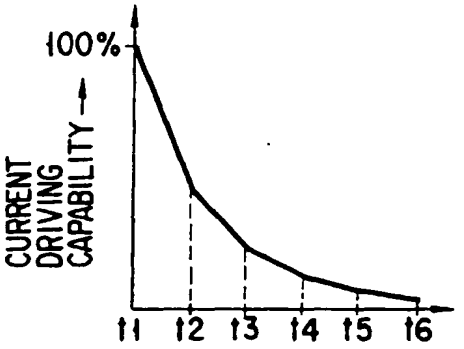


FIG. 10C



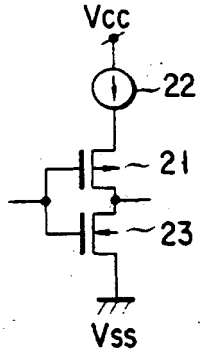


FIG. 11A

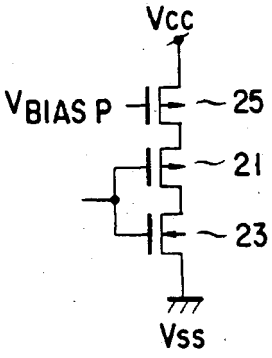


FIG. 11B

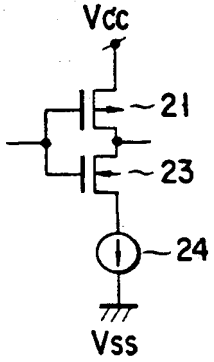


FIG. 12A

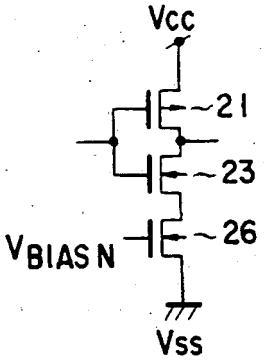


FIG. 12B

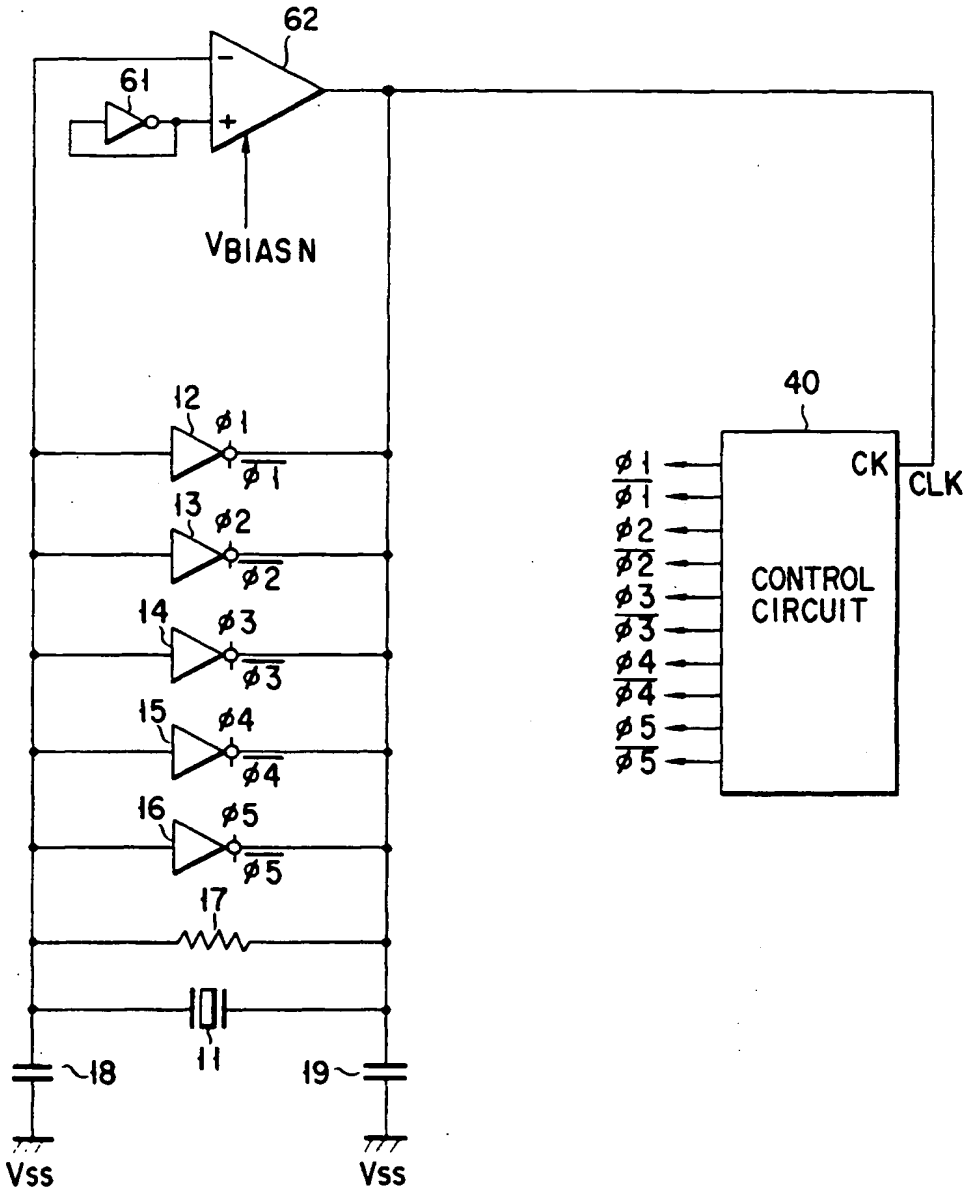

62
61
VBIASN
12
ø1
ø1
13
ø2
ø2
14
ø3
ø3
15
ø4
ø4
16
ø5
ø5
17
11
18
19
Vss
Vss
40
CK
CLK
ø1
ø1
ø2
ø2
ø3
ø3
ø4
ø4
ø5
ø5
CONTROL
CIRCUIT

FIG. 13

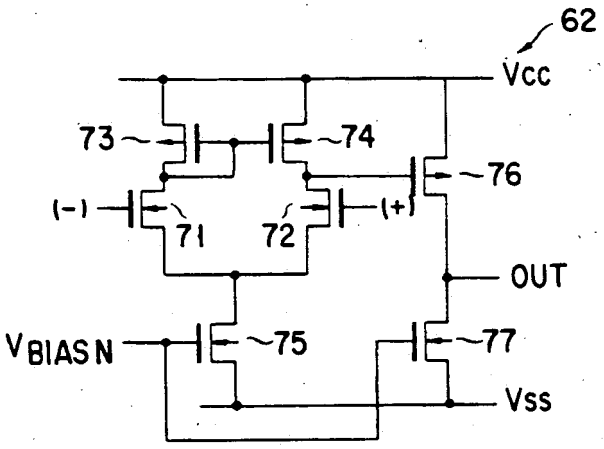

62
Vcc
73
74
76
(-)
71
72
(+)
OUT
VBIAS N
75
77
Vss

FIG. 14

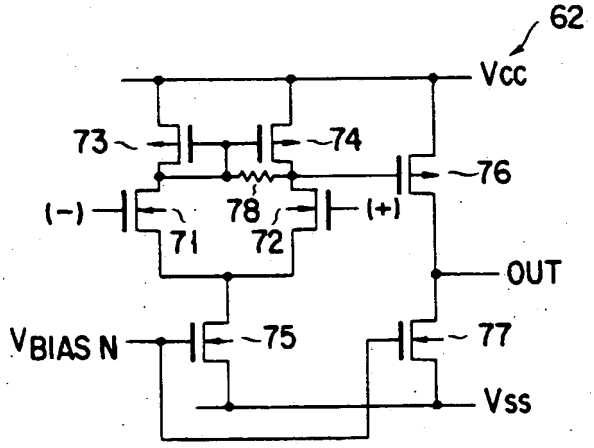

62
Vcc
73
74
76
(-)
78
(+)
71
72
OUT
VBIAS N
75
77
Vss

FIG. 15

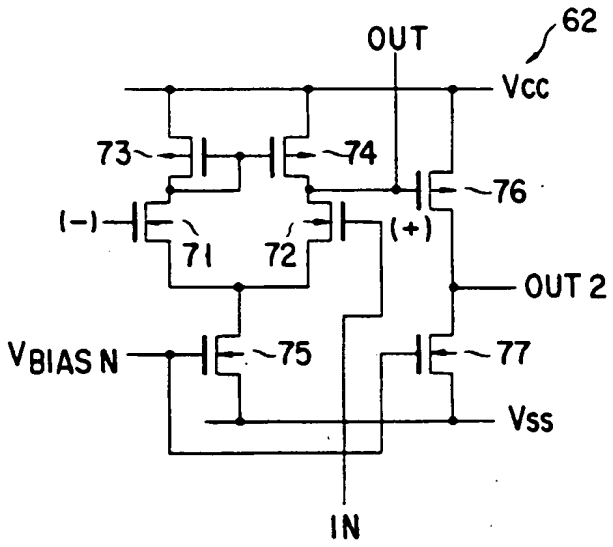


FIG. 16

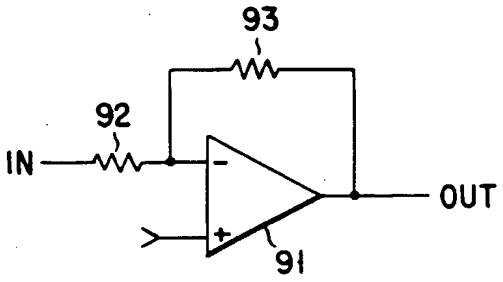


FIG. 17

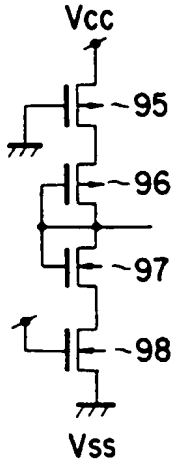


FIG. 18

DOCKET NO: P2001,0382

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APPLICANT: K.J. Feilkas et al.

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EUROPEAN PATENT OFFICE

Patent Abstracts of Japan

PUBLICATION NUMBER : 08065048
PUBLICATION DATE : 08-03-96

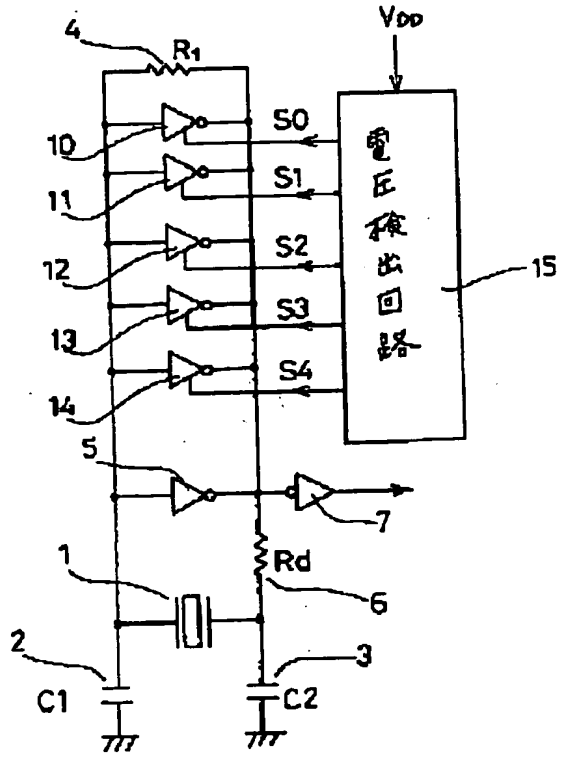
APPLICATION DATE : 22-08-94
APPLICATION NUMBER : 06196688

APPLICANT : SANYO ELECTRIC CO LTD;

INVENTOR : YAMAZAKI AKIRA;

INT.CL. : H03B 5/32

TITLE : OSCILLATION CIRCUIT



ABSTRACT : PURPOSE: To provide an oscillator for quickening an oscillation starting time during the rise of a power supply voltage, shortening an oscillation stable period after the power supply voltage reaches an operating voltage and suppressing the generation of higher harmonics as much as possible.

CONSTITUTION: In this oscillation circuit composed by connecting a first inverter 5 for which input and output are connected by a feedback resistor 4 parallelly to an oscillation vibrator 1, plural tristate inverters 11-14 or NAND gates are respectively parallelly connected to the first inverter 5, a voltage detection circuit 15 for detecting the voltage level of the power supply voltage to be supplied to the first inverter 5 is provided and the plural tristate inverters 11-14 are selectively turned to an operating state or the NAND gate is selectively opend/closed corresponding to the detecting voltage level.

DOCKET NO: P2001,0382

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APPLICANT: K.J. Feilkas et al.

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Patent Abstracts of Japan

PUBLICATION NUMBER : 04267607
PUBLICATION DATE : 24-09-92

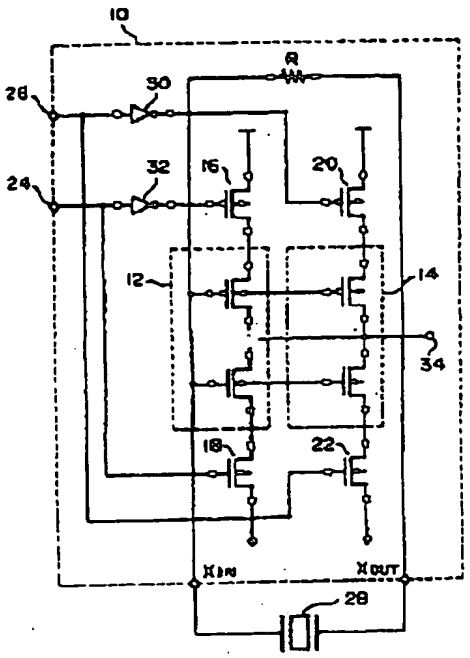
APPLICATION DATE : 21-02-91
APPLICATION NUMBER : 03048927

APPLICANT : NIPPON STEEL CORP;

INVENTOR : UKON ISAMU;

INT.CL. : H03B 5/32 G06F 1/06

TITLE : DRIVE CIRCUIT FOR OSCILLATION



ABSTRACT : PURPOSE: To minimize radiation noise corresponding to the oscillating frequency of a crystal oscillator in use.

CONSTITUTION: A different drive capability is given to inverters 12, 14 respectively and they act like drive sections. The inverter is selected depending on the oscillating frequency of a crystal oscillator 28 connecting to terminals XIN, XOUT. A signal to select the inverter is given from terminals 24, 26.

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DOCKET NO: P2001,0382
SERIAL NO: _____
APPLICANT: K.J. Feilkas et al.

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